



2829

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tawfik R. Arabi et al.
Title: AC TESTING OF LEAKAGE CURRENT

Docket No.: 884.410US1
Filed: April 19, 2001
Examiner: Russell Kobert

Serial No.: 09 838,730
Due Date: January 10, 2003
Group Art Unit: 2829

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

A return postcard.
 Response to Restriction Requirement (4 Pages).
 Clean Version of Amended Specification Paragraphs (1 pg.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 10 day of January, 2003.

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Signature

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(GENERAL)



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Title: AC TESTING OF LEAKAGE CURRENT

RESPONSE TO RESTRICTION REQUIREMENT
AND PRELIMINARY AMENDMENTCommissioner for Patents
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In response to the Restriction Requirement mailed December 10, 2002, Applicant elects without traverse, invention I, species 1 including claims 1-9. Applicant cancels claims 10-20 without prejudice or disclaimer, and reserves the right to reintroduce them in one or more divisional applications at a later date.

Please amend the application as follows:

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

The paragraph beginning on page 5, line 6 is amended as follows:

Pin to Vcc or Pin to Vss test

In general, at the beginning of the test, a pin is tri-stated or floated. The pin is subsequently driven to a known state with a Boundary Scan pattern (Vss, Vcc, low, or high) for a first predetermined time. After the pin reaches the known state, it is allowed to float or to be unconnected. If the pin has the defect being [test] tested for, it leaks and eventually changes from one state to the other state. At a second predetermined time, the pin is sampled with Boundary Scan. In other words, the voltage value of the pin is measured by internal circuitry of the IC to determine its state at the second predetermined time. Based on the state (measured voltage) of the pin, a pass fail result is determined. In the following detailed description, for simplicity, only leakage testing of pin 122-0 is described; other pins (122 1-N) are tested in the same manner. In one embodiment, only input output pins of IC 120 are tested with Boundary Scan.

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